## AMENDMENT TO THE CLAIMS

1. (Previously Presented) A host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising:

a processor;

a host memory coupled to said processor; and

a host-fabric adapter coupled to said processor and provided to interface with said switched fabric, including an internal cache to store selected translation and protection table (TPT) entries from said host memory for a data transaction, each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory, a translation cacheable flag to specify whether said host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory;

wherein said host-fabric adapter is configured to flush individual cached TPT entries from said internal cache in accordance with the corresponding translation cacheable flag.

2. (Cancelled)

3. (Previously Presented) The host as claimed in claim 1, wherein each of said selected TPT entries represents translation of a single page of said host memory.

4. (Previously Presented) The host as claimed in claim 1, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said selected TPT entries.

5. (Cancelled)

6. (Previously Presented) The host as claimed in claim 1, wherein said protection attributes comprise a Memory Write Enable flag to indicate whether said host-fabric adapter can write to a page; a RDMA Read Enable flag to indicate whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag to indicate whether the page can be a target of a RDMA Write operation.

7. (Previously Presented) The host as claimed in claim 1, wherein said host-fabric adapter flushes a designated cached TPT entry from said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a first logical state, and maintains said designated cached translation cacheable flag of said designated cached TPT entry in said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a second logic state opposite of said first logic state.

8. (Previously Presented) The host as claimed in claim 1, further comprising an operating system including driver software which sets status of said translation cacheable flag per TPT

entry for enabling said host-fabric adapter to flush individual cached TPT entry from said internal cache.

9. (Previously Presented) A network, comprising:

a switched fabric;

I/O controllers attached to said switched fabric; and

a host comprising an operating system, a host memory, and a host-fabric adapter including translation and protection table (TPT) entries, each TPT entry comprising protection attributes to control read and write access to a given memory region of the host memory, a translation cacheable flag to specify whether the host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether the host-fabric adapter has permission to access said host memory;

wherein the host-fabric adapter is configured to cache selected TPT entries from the host memory and to flush individual cached TPT entries in accordance with the corresponding translation cacheable flag.

10. (Previously Presented) The network as claimed in claim 9, wherein said host-fabric adapter comprises an internal cache to store said selected TPT entries from said host memory.

11. (Previously Presented) The network as claimed in claim 9, wherein each of said selected TPT entries represents translation of a single page of said host memory.

12. (Previously Presented) The network as claimed in claim 9, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said selected TPT entries.

13. (Cancelled)

14. (Previously Presented) The network as claimed in claim 9, wherein said protection attributes comprise a Memory Write Enable flag to indicate whether said host-fabric adapter can write to page; a RDMA Read Enable flag to indicate whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag to indicate whether the page can be a target of a RDMA Write operation.

15. (Previously Presented) The network as claimed in claim 10, wherein said host-fabric adapter flushes a designated cached TPT entry from said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a first logical state, and maintains said designated cached TPT entry in said internal cache for future re-use when said translation cacheable flag of said designated cached TPT entry indicates a second logic state opposite of said first logic state.

16. (Currently Amended) An apparatus, comprising:

a host-fabric adapter provided to interface with a switched fabric;

a storage device to store translation and protection table (TPT) entries for virtual to physical address translations, wherein each of said TPT entries include protection attributes to control read and write access to a given memory region of a host memory and a memory protection tag to specify whether said apparatus has permission to access said host memory; and

a mechanism to flush individual TPT entries stored in the storage device in accordance with a corresponding translation cacheable flag included in the individual TPT entry.

17. (Previously Presented) The apparatus as claimed in claim 16, wherein the storage device corresponds to an internal cache for storing said TPT entries.

18. (Previously Presented) The apparatus as claimed in claim 16, wherein each of said TPT entries represents translation of a single page of a host memory.

19. (Previously Presented) The apparatus as claimed in claim 17, wherein each of said TPT entries comprises:

said translation cacheable flag to specify whether said apparatus may flush a corresponding translation and protection table (TPT) entry stored in said internal cache; and

a physical page address field to address a physical page frame of data entry.

20. (Previously Presented) The apparatus as claimed in claim 19, wherein said protection attributes comprise a Memory Write Enable flag to indicate whether said apparatus can write to page; a RDMA Read Enable flag to indicate whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag to indicate whether the page can be a target of a RDMA Write operation.

21. (Currently Amended) A method, comprising:

storing, in a cache of an adapter installed in a host system and provided to interface a switched fabric, translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag and a memory protection tag to specify whether the adapter has permission to access the host memory; and

checking a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache of the adapter to determine whether to discard one or more selected TPT entries from the cache of the adapter wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache; and

a physical page address field which addresses a physical page frame of data entry.

22. (Previously Presented) The method as claimed in claim 21, further comprising a step of setting the status of the translation cacheable flag per TPT entry, using an operating system (OS), for enabling the adapter to discard individual TPT entries from the cache.

23. (Previously Presented) The method as claimed in claim 21, wherein each of the TPT entries represents translation of a single page of host memory.

24. (Cancelled).

25. (Previously Presented) The method as claimed in claim 21, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of a RDMA Write operation.

26. (Currently Amended) An adapter in a host system provided to interface a switched fabric, comprising:

a cache to store translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag and a memory protection tag to specify whether the adapter has permission to access the host memory; and

a mechanism to determine a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache, and to discard the one or more selected TPT entries from the cache based on the status of the translation cacheable flag wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache; and

a physical page address field which address a physical page frame of data entry.

27. (Previously Presented) The adapter as claimed in claim 26, further comprising an operating system (OS) to set the status of the translation cacheable flag per TPT entry for enabling the adapter to discard individual TPT entries from the cache.

28. (Previously Presented) The adapter as claimed in claim 26, wherein each of the TPT entries represents translation of a single page of host memory.

29. (Cancelled).

30. (Previously Presented) The adapter as claimed in claim 26, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be

a source of a RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of RDMA Write a operation.